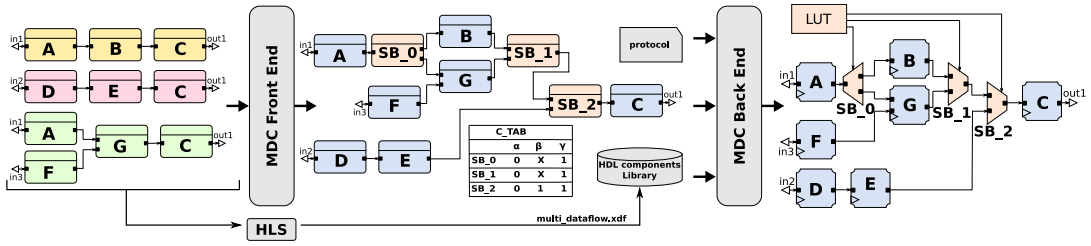
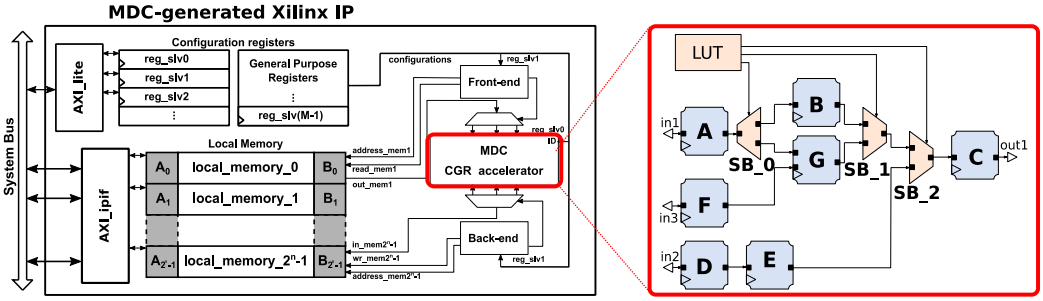
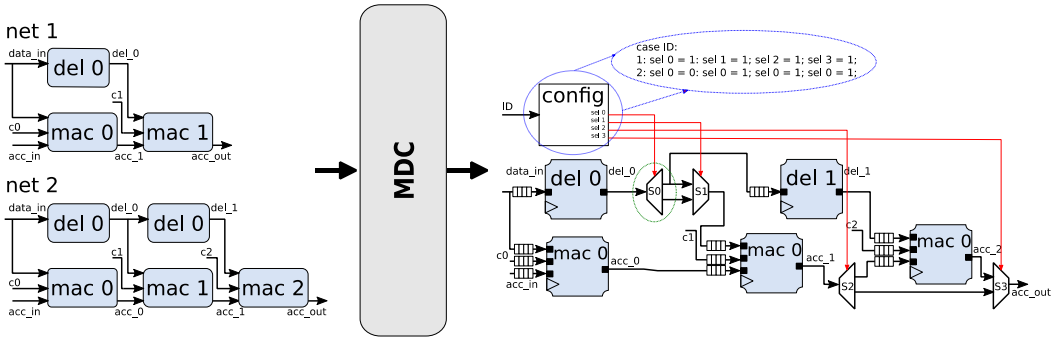
Users	• Software developers/embedded system engineers with little to none knowledge of the hardware • Hardware architects/embedded system engineers requesting for additional features (e.g. power optimization
Key Features	• composition of different high-level abstract functional specification to be implemented on a single accelerator, based on coarse-grained reconfigurable technologies • automatic resource minimization • automatic reconfiguration management
Benefits for the User	• design automation from high level models (dataflows) to hardware • handling of complex and time consuming design issues, such as topology exploration or power optimization • easy system integration within Xilinx platforms
Inputs	• high level models (dataflow) of functionalities to be implemented - XDF, Cal • HDL description of the components (HDL Components Library, HCL) corresponding to the dataflow actors, manually or automatically generated - Verilog, VHDL • hardware communication protocol between components - XML
Outputs	• (baseline) HDL description corresponding to the multi-functional model - Verilog, VHDL • (optional) multi-functional model resulting from the combination of the input applications models - XDF, Cal • (optional) Xilinx IP wrapper logic, scripts and drivers - XML, Verilog, Tcl, C
Block Design (baseline)	
Block Design (IP wrapping)	
Example Fir filters	 Example: Given 2 input dataflows (2-tap and a 3-tap FIR filters). Output: accelerator capable of switching among the filters. Four switching elements are inserted automatically to manage reconfiguration (configuration pattern size: 4 bits). APIs for filter delegation are provided.
Role in the	HW-Adaptivity support at the edge.

Toolchain	